Abstract — This paper presents the design of two low-voltage differential class-E power amplifiers (PA) for DECT and Bluetooth fabricated in 130nm CMOS. In order to minimize the on-chip losses and to achieve a high efficiency at low supply voltages, the PAs do not use on-chip output matching networks. At 1.5V supply voltage, the DECT PA delivers +26.4dBm of output power with a drain efficiency (DE) and power-added efficiency (PAE) of 41% and 30%, respectively. The Bluetooth PA delivers +22.7dBm at 1V with a DE and PAE of 48% and 36%, respectively. A continuous long-term test of 100 hours proves the reliability of the design.

Index Terms — CMOS, efficiency, power amplifier, reliability testing, frequency shift keying.

I. INTRODUCTION

The power amplifier (PA) is a key building block in all RF transmitters. Today, most radio frequency building blocks have been successfully integrated into CMOS processes, while the power amplifier is usually designed in a different technology. To lower the costs, by reducing board space and the number of components, it is highly desirable to integrate the entire transceiver and the PA in a single CMOS chip operated with a single low ‘digital’ supply voltage. Therefore, there is a need for highly efficient CMOS power amplifiers using a low supply voltage to achieve the goal of single-chip radio systems.

In this paper, we present two class-E CMOS PAs operating at a low ‘digital’ supply voltage. To achieve high efficiency and minimize on-chip losses, all output matching network components are put off-chip. Hence, low-Q on-chip inductors are avoided. Additionally, the integrated inductors commonly used for matching between the different amplifier stages are removed, which result in a significantly reduced area required for the PA.

A major obstacle in the design of class-E CMOS PAs is the high peak drain voltage generated, and the low breakdown voltage of the MOS device, making it challenging to design a reliable class-E CMOS PA. To evaluate the reliability of the design, a continuous long-term test of 100 hours has been performed. The paper discusses the design and implementation of the DECT and Bluetooth (BT) PAs including the circuit architecture, the experimental results, and eventually a comparison with other published low-voltage CMOS PA designs. The comparison shows a clear power-efficiency trade-off between the utilization of on-chip and off-chip output matching networks.

II. DESIGN AND IMPLEMENTATION OF THE POWER AMPLIFIERS

Both PAs utilize a differential structure (Fig. 1 shows a single-ended section) with buffers, and drivers based on 1.5V thin gate oxide transistors, with a physical gate oxide thickness (t ox) of 2.2nm, and gate length of 0.12µm, which are also used in the output stage (T 1 ) of the BT PA. The DECT PA utilizes 3.3V thick gate oxide (t ox )=5.2nm) transistors (T 1 ) with a gate length of 0.4µm.

Due to the relationship between DE, switch on-resistance (r on), and load resistance (R L ) in (1), it is important to reduce the on-resistance for high output power and high power efficiency [1]. Moreover, in order to achieve the same output power for a reduced power supply voltage [2], the load resistance needs to scale quadratically as in (2). Since the on-resistance does not reduce as fast as R L when technology scales, a low-voltage high-efficiency PA requires wider transistors in deep-submicron CMOS technologies [1].

\[
DE \propto \frac{1}{1 + 1.4 \frac{r_{on}}{R_L}} 
\]

\[
P_{out} = 0.577 \frac{V_{DD}^2}{R_L} 
\]

A simplified schematic of the PAs (single-ended section)
To benefit from the low on-resistance of the wider transistors, the parasitic inductance and resistive losses in the ground plane must be minimized. This is done by maximizing the number of metal layers used as ground, especially around the output stage transistors. However, as the size of the output stage transistor becomes larger, the capacitive loading of the buffer increases, and therefore a buffer with high driving capability is required.

The signal driving the PA is buffered with a buffer-chain consisting of regular inverters optimized to achieve a high overall efficiency. It means a trade-off between providing a good edge-rate on the gate of the following inverter to minimize the short-circuit current and not consume too much power. Fig. 1 shows the tapered buffer with a load capacitance \( C_L \) representing the gate capacitance of the output stage transistor and drain capacitance of the previous inverter stage. For a four-stage buffer with a tapering factor of three, the power dissipation of the last driver theoretically consumes two thirds of the total power consumption of the driver stages [3]. In order to achieve a good edge-rate at the output, the gate resistance is minimized by using a small finger gate width of 10\( \mu \)m for the BT PA. To achieve the required output power for DECT a wider transistor was needed, but to get reasonable layout proportions of the output stage, a finger width of 30\( \mu \)m was used in the output stage.

As the transistors become large, the drain capacitance increases and can be incorporated in the required capacitance \( C_L \) for class-E operation. However, it is important to minimize the voltage across the capacitance as the transistor is turned on, in order to minimize the energy losses.

In the implemented DECT and BT PAs the output power level can be adjusted by controlling the supply voltages of the output stage and driver stages of the PAs. Therefore, a voltage modulator will be needed for power control.

In Fig. 1, the NMOS transistor widths (in \( \mu \)m) of the three inverter driver stages and the output stage \( (T_{1} \) in Fig. 1) of the DECT PA are 100, 400, 1200, and 8400. The NMOS transistor widths of the four inverter driver stages and the output stage of the BT PA are 100, 200, 600, 1300, and 4000. The PMOS transistors were a factor of 2.2 larger.

III. EXPERIMENTAL RESULTS

Fig. 2 shows the photographs of the fabricated PAs, with the output stage at the top in the photos. The size of the chips is 0.7x1.2 mm\(^2\) and were directly bonded on the PCB (FR4, \( e_r = 4.2 \), \( \tan \delta = 0.035 \)). The input power was applied differentially with an external balun connected to the signal source. The PA utilizes an off-chip lumped element balun [4] for differential-to-single-ended conversion and load impedance transformation.

A. Measurement Results – Output Power

Fig. 3 shows how the output power of the DECT PA varies as the supply voltages (VDD\(_1\) and VDD\(_2\)) are swept from 0.8V to 1.5V. The highest output power is +26.4dBm at 1.5V with DE and PAE of 41% and 30%, respectively. As seen in Fig. 4, the performance of the PA varies over frequency, with an optimum performance at 1.85GHz when the supply voltage is 1.5V.

Fig. 5 shows how the output power of the BT PA varies as the supply voltage (VDD\(_1\)) is swept from 0.1V to 1.1V, with a maximum output power of +23.5dBm at 1.1V. At 1V the output power is +22.7dBm with DE and PAE of 48% and 36%, respectively. The buffers and the drivers use a 1V supply voltage. As seen in Fig. 6 the performance of the PA varies over frequency, but has an optimum performance at 2.45GHz for a 0.75V supply voltage. The

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**Fig. 2.** Chip photos: DECT (a) PA and Bluetooth (b) PA

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B. Measurement Results – Spectral Requirements

In Fig. 7 the measured output spectrums of the GFSK modulated signals for the DECT and BT PAs are seen. Based on the measured output spectrum and ACP calculations, the DECT PA meets the ACP requirements that are for channel offsets of ±1, ±2, ±3, and any other channel (±4). The Bluetooth PA meets the spectral mask requirement of -20dBc at an offset of ±500kHz, and ACP requirements of -20dBm, and -40dBm, for channel offsets of ±2, and ±3.

C. Measurement Results – Reliability

Since the drain voltage of a class-E PA ideally can reach levels up to 3.56xVDD [2], a low supply voltage is needed to minimize the stress on the output stage transistors and to not exceed the critical gate oxide field of ~1V/nm [2] for DC conditions. The damages in PAs are mainly due to channel hot carrier (HC) stress [6] or Fowler-Nordheim (F-N) gate oxide wearout [7]. Typically in a class-E PA, the drain voltage is high when the drain current is zero, and therefore the HC stress is minimized and the transistor wearout will be dominated by the F-N gate oxide wearout.

Simulations of both PAs indicate that the peak drain voltage reaches levels close to 3xVDD. As the DECT PA uses thick gate oxide transistors ($t_{ox}=5.2nm$) and a maximum supply voltage of 1.5V, the peak drain voltage is ~4.5V (~1V/nm). In the technology used, the thick gate oxide transistor can withstand voltages of ~8.5V for zero current (typical Class-E behavior), and a reasonable lifetime of the device can be expected.

In order not to exceed the critical gate oxide field in the BT PA a supply voltage of 0.75V has to be used for the thin gate oxide transistors ($t_{ox}=2.2nm$) in the output stage. However, the thin gate oxide NMOS transistor of the technology used, can withstand voltages of ~4.5V for zero current, indicating that a higher supply voltage can be used. To estimate the lifetime of the PA, one device was operated at 1V with output power of 22.7dBm. The device showed no output power level degradation after 100 hours of operation with 100% duty-cycle, however a minor increase of drain current was observed similar to [8].

D. Measurement Results – Performance Comparison

Table 1 shows the performance of the DECT PA and two recently presented DECT PAs [9], which are also designed in the same CMOS technology and also use off-chip output matching network, however both designs feature linear amplification. The PA shows a slightly lower output power and efficiency, while delivering a sufficiently high output power to leave some margin for output matching network losses to have +24dBm [9] at the antenna. It can be concluded that the supply voltage is reduced by 40% compared to [9], and the area has been reduced by approximately 91-93%, as seen in Table 1.

Our BT PA is the only PA achieving +20.4dBm of output power from a supply voltage as low as 0.75V compared to [5], [6], [10]-[12] in Table 1, however it does not have on-chip output matching networks as [5], [11], and needs a voltage supply modulator for linear power amplification. At 1V and +22.7dBm output power, the PA has a similar [12] or higher [5], [11], efficiency, even if the supply voltage is reduced by ~33% [5], [12] or by ~60%
Compared to the state-of-the-art 1-1.5V CMOS PAs [5], [13], [14], which use on-chip power combiners, the BT PA achieves almost double DE [13], [14] at output power levels of 23-24dBm, and a higher overall efficiency than [5] at a reduced supply voltage.

IV. SUMMARY

Two low-voltage class-E power amplifiers in 130nm CMOS intended for DECT and Bluetooth have been presented. At 1.5V supply voltage, the DECT PA manages to deliver +26.4dBm with a DE of 41% and PAE of 30%. The Bluetooth PA shows reliable operation at a supply voltage of 1V at an output power of +22.7dBm with DE, and PAE of 48%, and 36%, respectively. In comparison with other low-voltage CMOS PAs, the design shows a clear power-efficiency trade-off between the utilization of on-chip and off-chip output matching networks. The Bluetooth power amplifier device was operated for 100 hours with no output power level degradation.

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REFERENCES


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* Including inductors/transformers, tuning capacitors (not decoupling), and transistors (W×L).